

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT		Docket Number 02885/77	
Application Number To be assigned	Filing Date Herewith	Examiner To be assigned	Art Unit To be assigned
Invention Title METHOD OF HIERARCHICAL CACHING OF CONFIGURATION DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING TWO- OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAs, DPGAs, etc.)		Inventor(s) VORBACH et al.	

Address to:
 Mail Stop Patent Application
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicants hereby bring the following references to the attention of the Examiner. The references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.
2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is not enclosed (unless otherwise noted) since they were previously cited by or submitted to the Patent Office in prior applications Serial No. 10/191,926, filed **July 9, 2002**, and 09/623,052, filed **January 9, 2001**, which are relied upon for an earlier filing date under 35 U.S.C. 120.

Dated: 23 Jan 2001

By:



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Form PTO-1449	ATTY. DOCKET NO. 02885/77	SERIAL NO. To be assigned
	APPLICANT VORBACH et al.	
	FILING DATE Herewith	GROUP To be assigned

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EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
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	4,706,216	November 10, 1997	Carter			
	4,739,474	April 1, 1988	Holsztynski			
	4,761,755	August 2, 1998	Ardini, et al.			
	4,811,214	May 7, 1989	Nosenchuck et al.			
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	196 54 595	July 2, 1998	Germany			X	
	196 54 846	July 9, 1998	Germany			X	
	197 04 728	August 13, 1998	Germany			X	
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	0 726 532	August 14, 1996	Europe			X	
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	0 539 596A1	May 5, 1993	Europe			X	
	735 685	October 2, 1996	Europe			X	
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	44 16 881	November 17, 1994	Germany			X	
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		M. Saleeba, "A Self-Contained Dynamically Reconfigurable Processor Architecture", Sixteenth Australian Computer Science Conference, ASCS-16, QLD, Australia, February, 1993.
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		*Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic," IEEE, 1996, pp 126-135
		*Cadambi et al., "Managing Pipeline-Reconfigurable FPGAs," ACM, 1998, pp 55-64

*Reference cited by Examiner in a prior application

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	